Amendments to the Specification:

Please replace the paragraph beginning at page 5, line 5, with the following redlined paragraph:

Figure 6 shows a schematic diagram of a 2-to-4 decoder in accordance with the invention. ~~For~~ for the case when the inputs $\overline{A}B$ and AB. When the inputs are A = 0, B = 1, transistors 6.6 is in conducting state and pulls Y1 to LOW. This causes transistor 6.2 to conduct pulling Y3 HIGH. Similarly, when the inputs are A = 1, B = 1, transistor 6.3 is in conducting state and pulls Y3 to LOW. This results in transistor 6.4 conducting and pulling Y1 HIGH.

Please replace the paragraph beginning at page 5, line 11, with the following redlined paragraph:

Figure 7 shows a schematic diagram of a 3-to-8 decoder in accordance with the invention. ~~For~~ for the case when the inputs are $\overline{A}\overline{B}\overline{C}$ and $A\overline{B}\overline{C}$. When the inputs are A = 0, B = 0, C = 0 transistors 7.8 and 7.9 are in conduction pulling Y0 LOW. This sets transistor 7.3 conducting pulling Y4 HIGH. Similarly, when the inputs are A = 1, B = 0, C = 0, transistors 7.4 and 7.9 are in conduction and Y4 is pulled LOW. This sets transistor 7.5 conducting, pulling Y0 HIGH.

Please replace the paragraph beginning at page 5, line 17, with the following redlined paragraph:

Figure 8 shows a schematic diagram of a 3-to-8 decoder in accordance with the invention. ~~For~~ for the case when the inputs are $\overline{A}\overline{B}C$ and $A\overline{B}C$. When the inputs are A = 0, B = 0, C = 1 transistors 8.8 and 8.9 are in conduction and pull Y1 LOW. This sets transistor 8.3 conducting, pulling Y5 HIGH. When the inputs are A = 1, B = 0, C = 1 transistors 8.4 and 8.9 are in a conducting state, pulling Y5 LOW. This sets transistor 8.5 conducting, pulling Y1 HIGH.

Please replace the paragraph beginning at page 5, line 23, with the following redlined paragraph:

Figure 9 shows a schematic diagram of a 3-to-8 decoder in accordance with the invention. ~~For~~ for the case when the inputs are $\overline{A}B\overline{C}$ and $AB\overline{C}$. When the inputs are A = 0, B = 1, C = 0 transistors 9.8 and 9.9 are in conduction pulling Y2 LOW. This sets transistor 9.3 conducting, pulling Y6 HIGH. Similarly, when the inputs are A = 1, B = 1, C = 0, transistors 9.4 and 9.9 are in a conducting state, pulling Y6 LOW. This sets transistor 9.5 conducting, pulling Y2 HIGH.

Please replace the paragraph beginning at page 6, line 1, with the following redlined paragraph:

Figure 10 shows a schematic diagram of a 3-to-8 decoder in accordance with the invention. ~~For~~ for the case when the inputs are $\overline{A}BC$ and ABC. When the inputs are A = 0, B = 1, C = 1, transistors 10.8 and 10.9 are in a conducting state, pulling Y3 LOW. This sets transistor 10.3 conducting pulling Y7 HIGH. Similarly, when the inputs are A = 1, B = 1, C = 1, transistors 10.4 and 10.9 are in conduction, pulling Y7 LOW. This sets transistor 10.5 conducting pulling Y3 HIGH.

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) An improved binary decoder, comprising:

selection means for activating from a plurality of outputs a selected output corresponding to an input binary value, and

deselecting means coupled to ~~each output~~ the plurality of outputs that deactivates ~~all other~~ the plurality of outputs except the selected output when the selected output is activated.

2. (Original) The improved binary decoder of claim 1, wherein the selection means comprises a circuit arrangement of gates for selecting a desired output.

3. (Original) The improved binary decoder of claim 1, wherein the deselecting means comprises a circuit arrangement having a single input connected to the selected output of the selection means, and a plurality of outputs each of which is connected to one of the remaining outputs of the selection means, such that when the input of the circuit arrangement is active all the other outputs of the decoder are forced to the inactive state.

4. (Currently Amended) A method for providing an improved binary decoder, comprising the steps of:

providing selection means for activating from a plurality of outputs a selected output corresponding to ~~the~~ an input binary value, and

providing a deselecting means coupled to ~~each output~~ the plurality of outputs for deactivating ~~all other~~ the plurality of outputs of the selection means except the selected output when the selected output is activated.

5. (Previously Presented) A binary decoder, comprising:

a first pair of parallel-coupled transistors and a second pair of parallel-coupled transistors, the first and second pair of parallel-coupled transistors coupled between a voltage source and first and second outputs, respectively;

a third transistor coupled between the first output and a reference potential, and a fourth transistor coupled between the second output and the reference potential; and

the first and second pair of parallel-coupled transistors each having an input terminal, and the third and fourth transistors each having an input terminal, the first output coupled to a first input of the second pair of parallel-coupled transistors, the second output coupled to a first input of the second pair of parallel-coupled transistors.

6. (Previously Presented) The decoder of claim 5, wherein the input terminals of the first and second pair of parallel-coupled transistors are each configured to receive a compliment of a first input signal, the input terminal of the third transistor configured to receive the compliment of a second input signal and the input terminal of the fourth transistor configured to receive the uncomplimented first input signal.

7. (Previously Presented) The decoder of claim 5, wherein the input terminals of the first and second pair of parallel-coupled transistors are each configured to receive the uncomplimented input of a first input signal, the third transistor having its input terminal configured to receive the compliment of a second input signal, and the fourth transistor having its input terminal configured to receive the uncomplimented second input signal.

8. (Previously Presented) A decoder for integrated circuits, comprising:

a first set of parallel-coupled transistors coupled between a voltage source and a first output and comprising first, second, and third transistors, each having respective inputs;

a second set of parallel-coupled transistors coupled between the voltage source and a second output, the second set of parallel-coupled transistors comprising fourth, fifth, and sixth transistors, each having respective inputs;

a seventh transistor coupled between the first output and a common node and having an input, an eighth transistor coupled between the second output and the common node and having an input, and a ninth transistor coupled between the common node and a voltage reference and having an input.

9. (Previously Presented) The decoder of claim 8, wherein the input of the first transistor is coupled to the second output, the input of the third transistor is coupled to the second output, the input of the seventh transistor is configured to receive an uncomplimented first input signal, the input of the eighth transistor is configured to receive the compliment of the first input signal, the input of the second transistor configured to receive the compliment of a second input signal, the input of the third transistor configured to receive the compliment of a third input signal, the input of the fifth transistor configured to receive the compliment of the second input signal, the input of the sixth transistor configured to receive the compliment of the third input signal, the input of the ninth transistor configured to receive the compliment of the second input signal, and the reference potential set to the uncomplimented third input signal.

10. (Previously Presented) The decoder of claim 8, wherein the first and second outputs are set to active low.

11. (Previously Presented) The decoder of claim 8, wherein the input of the first transistor is coupled to the second output, the input of the fourth transistor is coupled to the first output, the input of the seventh transistor is configured to receive an uncomplimented first input signal, the input of the eighth transistor configured to receive the compliment of the first input signal, the input of the second transistor configured to receive the compliment of the second input signal, the input of the third transistor configured to receive an uncomplimented third input signal, the input of the fifth transistor configured to receive the compliment of the second input signal, the input of the sixth transistor configured to receive the uncomplimented third input signal, the input of the ninth transistor configured to receive the complimented input of the second input signal, and the reference potential set to the complimented third input signal.

12. (Previously Presented) The decoder of claim 8, wherein the input of the first transistor is coupled to the second output, the input of the fourth transistor is coupled to the first output, the input of the seventh transistor is coupled to an uncomplimented first input signal, the input of the ninth transistor is coupled to an uncomplimented second input signal, the input of the second transistor is coupled to a complimented third input signal, the third transistor is coupled to an uncomplimented second input signal, the fifth transistor is coupled to the second uncomplimented input signal, the sixth transistor is coupled to the complimented third input signal, and the ground reference is set to the uncomplimented third input signal.

13. (Previously Presented) The decoder of claim 8, wherein the input of the first transistor is coupled to the second output, the input of the fourth transistor is coupled to the first input, the input of the seventh transistor is coupled to an uncomplimented first input signal, the input of the second transistor is coupled to an uncomplimented second input signal, the input of the third transistor is coupled to an uncomplimented third input, the input of the fifth transistor is coupled to the uncomplimented second input signal, the input of the sixth transistor is coupled to the uncomplimented third input signal, the input of the eighth transistor is coupled to the complimented first input signal, the input of the ninth transistor is coupled to the uncomplimented second input signal, and the reference voltage set to the complimented third input signal.

14. (Currently Amended) The decoder of claim 8, wherein the first and second pair of parallel-coupled transistors comprises ~~PTMOS~~ PMOS transistors, and the third and fourth transistors comprise NMOS transistors.

15. (New) A binary decoder, comprising:

a selection circuit structured to activate from a plurality of outputs a selected output corresponding to an input binary value; and

a deselecting circuit coupled to the plurality of outputs that deactivates the plurality of outputs except the selected output when the selected output is activated.

16. (New) The binary decoder of claim 15, wherein the selection circuit comprises an arrangement of gates for selecting a desired output.

17. (New) The decoder of claim 15, wherein the deselecting circuit comprises a single input connected to the selected output of the selection circuit, and a plurality of outputs, each of which is connected to one of the remaining outputs of the selection circuit such that when the input of the deselection circuit is active, all the other outputs of the decoder are forced to an inactive state.

18. (New) The decoder of claim 15, wherein the selection and deselection circuits are connected to provide a 2-to-4 decoder that provides an active low output for an input of A'.B' and for an input A.B'.

19. (New) The decoder of claim 15, wherein the selection and deselection circuits are connected to provide a 2-to-4 decoder that provides an active low output for an input of A'.B and for an input A.B.

20. (New) The decoder of claim 15, wherein the selection and deselection circuits are connected to provide a 3-to-8 decoder that provides an active low output for an input of A'.B'.C' and for an input A.B'.C'.

21. (New) The decoder of claim 15, wherein the selection and deselection circuits are connected to provide a 3-to-8 decoder that provides an active low output for an input of A'.B'.C and for an input A.B'.C.

22. (New) The decoder of claim 15, wherein the selection and deselection circuits are connected to provide a 3-to-8 decoder that provides an active low output for an input of A'.B.C' and for an input A.B.C'.

23. (New) The decoder of claim 15, wherein the selection and deselection circuits are connected to provide a 3-to-8 decoder that provides an active low output for an input A'.B.C and for an input A.B.C.

24. (New) The decoder of claim 15, wherein the selection circuit includes:

a first transistor coupled between a reference voltage and a first one of the outputs; and

a second transistor coupled between the reference voltage and a second one of the outputs, wherein the deselection circuit includes:

a third transistor connected between the reference voltage and the first output and having an input connected to the second output: and

a fourth transistor connected between the reference voltage and the second output having an input connected to the first output.